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10/688,828	10/17/2003	Paul A. Farrar	MI22-2054	2370

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/688,828	FARRAR, PAUL A.
	Examiner	Art Unit
	Thong Q. Le	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-35* is/are allowed.

6)☒ Claim(s) *1-6,8-10,36-41 and 43-46* is/are rejected.

7)☒ Claim(s) *7 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-46 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/17/2003.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. Claims 11-16, 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 11 recites the limitation "the bitline" in line 11. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 16 recites the limitation "the bitline" in line 2. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 31 recites the limitation "the bitline" in line 9. There is insufficient antecedent basis for this limitation in the claim.

9. Regarding claim 11, lines 11, should be change "the bitline" to –the common bitline—as defined in line 9.

10. Regarding claim 16, line 2, should be change "the bitline" to –the common bitline—as defined in line 9 in claim.

11. Regarding claim 31, line 6, should be change "the bitline" to –the common bitline—as defined in line 9 in claim 31.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-6,8-10,36-41,43-46 are rejected under 35 U.S.C. 102(B) as being anticipated by Hieda et al. (U.S. Patent No. 5,106,774)

Regarding claim 1, Hieda et al. disclose a digital data apparatus (Figure 2) comprising:

a semiconductive substrate (ABSTRACT) comprising a node location (Figure 1, 18a) configured to receive an electrical charge of a single bit of digital information (Figure 1, 38, Column 4, lines 62-65) ;

a first capacitor (Figure 1, 20) coupled with the node location and configured to store a first portion of electrical charge of single bit of digital information (Figure 1, 38), wherein the first capacitor comprises a first type of capacitor structure (ABSTRACT, Column 2, lines 22-35, first capacitor is stacked transistor) ;

a second capacitor (Figure 1, 18a) coupled with the node location and configured to store a second portion of the electrical charge of the single bit of digital information, wherein the second capacitor comprises a second type of capacitive structure different than the first type of capacitive structure (ABSTRACT, Column 2, lines 22-35, second capacitor is trench capacitor); and

a transistor (Column 2, lines 25-26) coupled with the node location and configured to control a flow of the first and second portions of the electrical charge of the single bit of digital information with respect to the node location and respective ones of the first and the second capacitors (Figure 2 Q1, Column 2, lines 20-35, Column 4, lines 43-59).

Regarding claim 2, Hieda et al. disclose wherein a substantial portion of a storage component of the first capacitor (Figure 2, 20) is elevationally above a horizontal reference line and a substantial portion of a storage component of the second capacitor is elevationally below the horizontal reference line (Figure 2, 18a, first capacitor 20 is above and second capacitor 18 is below).

Regarding claim 3, Hieda et al. disclose wherein the horizontal reference line comprises a surface of semiconductive substrate (ABSTRACT).

Regarding claim 4, Hieda et al. disclose wherein the first type of capacitive structure comprises a stacked capacitor, and the second type of capacitive structure comprises a trench capacitor (ABSTRACT, Column 4, lines 12-32).

Regarding claim 5, Hieda et al. disclose wherein the first and second capacitors comprise a cell configured to store the single bit digital information (Column 4, lines 38-42, memory cell).

Regarding claim 6, Hieda et al. disclose a common bitline (Figure 1, 38), and wherein both of the first and the second capacitors are coupled with the common bitline via the transistor (Figure 1, bitline 38 coupled to gate 24 of a transistor and capacitors 18 and 20, Figure 2).

Regarding claim 8, Heida et al. disclose comprising processing circuitry (Figure 15, 114) coupled with the bitline (Figure 15, BL) and configured to control a content of the single bit of digital information comprising one of a plurality of logical states.

Regarding claims 9-10, Heida et al. disclose processing circuitry configured to access the single bit of digital information from the first and the second capacitors, and to control writing of the single bit of digital information to the first and the second capacitors (Figure 15, sense amplifier to use read and from a memory cell, column 12, lines 50-64).

Regarding claim 36, Heida et al. disclose a digital data operational (Figure 15) method comprising: providing a plurality of capacitors comprising a plurality of different types of capacitive structures using a semiconductive substrate (ABSTRACT, Figure 1, 18, 20);

communicating an electrical charge corresponding to a single bitline, of digital information using a bitline (Figure 1, 38);

storing the electrical charge of the single bit of digital information using plural ones of the capacitors comprising different types of capacitive structures (ABSTRACT, stacked capacitor and trench capacitor); and

controlling communication (figure 15, 114) of the electrical charge intermediate the capacitors and the bitline (Figure 15, BL) using a transistor to read and write the bit of digital information with respect to the capacitors.

Regarding claim 37, Heida et al. disclose wherein one of the capacitors (Figure 2, 20) is formed elevationally above a horizontal reference line and another of the capacitors (Figure 2, 18) is formed elevationally below the horizontal reference line.

Regarding claim 38, Heida et al. disclose wherein the one capacitor comprises a stacked capacitor and the other capacitor comprises a trench capacitor (ABSTRACT).

Regarding claim 39, Heida et al. disclose accessing the bit of digital information using processing circuitry (Figure 15, 114) configured to process the bit of digital information.

Regarding claim 40, Heida et al. disclose a digital data operational (Figure 15) method comprising providing a plurality of capacitors (Figure 1, 18, 20) comprising different types of capacitive structures (ABSTRACT) using a semiconductive substrate (ABSTRACT), communicating a plurality of electrical charges using a common bitline (Figure 1, 38) coupled with the capacitors (Figure 1, 18, 20), storing one of the electrical charges from the bitline using one of the capacitors having a first type of capacitive

structure, and storing an other of the electrical charges from the bitline using an other of the capacitors having a second type of capacitive structure different than the first type of capacitive structure (Figure 2, stacked capacitor 20 and trench capacitor 18).

Regarding claim 41, Heida et al. disclose wherein the one and the other electrical charges together comprise a single bit of digital information (Figure 1, 38, Column 4, lines 63-64).

Regarding claim 43, Heida et al. disclose wherein the providing comprises providing the one capacitor elevationally above a horizontal reference line and providing the other capacitor elevationally below the horizontal reference line (Figure 2, capacitor 20 above, capacitor 18 below).

Regarding claim 44, Heida et al. disclose wherein the one capacitor comprises a staked capacitor and the other capacitor comprises a trench capacitor (Figure 2, 20, 18, ABSTRACT).

Regarding claim 45, Heida et al. disclose wherein the storings of one and the other electrical charges individually comprise storing using a respective one of a plurality of transistors (Figure 2, Q1, Q2), and wherein one of the transistors is formed adjacent a sidewall of the other capacitor comprising a trench capacitor (Figures 1, 2).

Regarding claim 46, Heida et al. disclose processing the electrical charge using processing circuitry (figure 15, 114).

Allowable Subject Matter

14. Claims 7, 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7; 42 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Chung (U.S. Patent No. 6,031,774), and others, does not teach the claimed invention having a first capacitor comprise a pair of capacitor as claim 7 disclosed, and wherein the one and the other electrical charges comprise respective different bits of digital information as claim 42 disclosed..

15. Claims 11-16, 35 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

16. Claims 11-16, 35 are allowed.

Claims 11-16, 35 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Heida et al. (U.S. Patent No. 5,106,774), and others, does not teach the claimed invention having a plurality of transistors formed using the semiconductive substrate and coupled with the bitline, wherein the transistors are individually configured to control storage of a respective one of the first and the second electrical charges with respect to a respective one of the first and the second capacitors.

17. Claims 17-30 are allowed.

Claims 17-30 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Heida et al. (U.S. Patent No. 5,106,774), and others, does not teach the claimed invention having a plurality of transistors formed using the semiconductive substrate and individually associated with one of the first capacitor and second capacitor.

18. Claims 31-34 are allowed.

Claims 11-34 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Heida et al. (U.S. Patent No. 5,106,774), and others, does not teach the claimed invention having a control means for selectively communicating respective ones of the first and second electrical charges with respective ones of the first storage means and second storage means.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

4/7/2006